[0251] In each of the SiC semiconductor devices according to the sixth to ninth embodiments, the stripe portions of the P type deep layer **310** are formed along the approximately normal direction of the sidewall of the trench **306**, as an example. The P type deep layers **310** may also be formed along a direction inclined to the sidewall of the trench **306**. Alternatively, a part of the P type deep layers **310** may be arranged in a direction inclined to one side from the normal direction of the sidewall of the trench **306** and the other part of the P type deep layers **310** may be arranged in a direction inclined to the opposite side of the one side from the normal direction. In the present case, the part of the P type deep layers **310** cross the other part of the P type deep layers **310**, and thereby the P type deep layers **310** are arranged in a lattice pattern. At least the longitudinal direction of the P type deep layers **310** is set so as to cross the longitudinal direction of the trench **306**. That is, when the trench **306** is provided along a first direction, the P type deep layers **310** are formed along a second direction crossing the first direction. Also in these cases, the clearance between the P type deep layer **310** and the P type RESURF layer **315** described in the seventh embodiment and the dimension of the openings **310***a* described in the eighth embodiment are set to be less than the intervals of the stripe portions of the P type deep layer **310**.

[0252] In each of the SiC semiconductor devices according to the sixth to ninth embodiments, the peripheral high-voltage part is configured by the P type RESURF layer **315** and the P type guard ring layers **316**. However, a configuration of the peripheral high-voltage part is not limited to the above-described example. The peripheral high-voltage part may be a general peripheral high-voltage structure. Also in the present case, the outer edge portion of the P type deep layer **310** can be formed at the whole area of the outer edge portion of the cell section Sa as described in the sixth embodiment, the outer edge portion of the P type deep layer **310** can be away from the peripheral section Sb as described in the seventh embodiment, or the openings **310***a* can be provided at the outer edge portion of the P type deep layer **310**. By forming the P type deep layer **310** at the outer edge portion of the cell section Sa, a portion where a breakdown can possibly occur is moved to the peripheral section Sb. Thus, the breakdown voltage can be increased.

[0253] Each of the SiC semiconductor devices according to the sixth to ninth embodiments includes the MOSFETs having the inversion type trench gate structure, as an example. Alternatively, each of the SiC semiconductor devices according to the sixth to ninth embodiments may include a MOSFET having an accumulation type trench gate structure as illustrated in FIG. **40**. In the present case, an N− type channel layer **320** disposed in the trench **306** and the gate electrode **309** is disposed on a surface of the N− type channel layer **320** through the gate oxide layer **308**.

[0254] When an orientation of a crystal face is described, it is originally required for attaching a bar above a desired figure. However, the bar is attached before the figure in the present application.

What is claimed is:

1. A silicon carbide semiconductor device comprising:

a substrate made of silicon carbide, the substrate having one of a first conductivity type and a second conductivity type, the substrate having first and second opposing surfaces;

a drift layer located on the first surface of the substrate, the drift layer made of silicon carbide, the drift layer having the first conductivity type and having an impurity concentration less than an impurity concentration of the substrate;

a trench provided from a surface of the drift layer;

a gate insulating layer located in the trench;

a base region sandwiching the trench, the base region having a predetermined distance from the gate insulating layer on a sidewall of the trench, the base region made of silicon carbide and having the second conductivity type;

a channel layer located between the base region and the gate insulating layer, the channel layer made of silicon carbide and having the first conductivity type;

a source region located on the base region and sandwiching the trench, the source region being in contact with the channel layer, the source region made of silicon carbide, the source region having the first conductive type and having an impurity concentration greater than the impurity concentration of the drift layer;

a gate electrode located on the gate insulating layer in the trench;

a source electrode electrically coupled with the source region and the base region;

a drain electrode located on the second surface of the substrate; and

a deep layer located under the base region and extending to a depth deeper than the trench, the deep layer formed along an approximately normal direction to the sidewall of the trench, the deep layer having the second conductivity type, wherein

an accumulation channel is provided at the channel layer on the sidewall of the trench and electric current flows between the source electrode and the drain electrode through the source region and the drift layer by controlling a voltage applied to the gate electrode.

2. The silicon carbide semiconductor device according to claim **1**, wherein

the deep layer has an impurity concentration greater than or equal to an impurity concentration of the base region.

3. The silicon carbide semiconductor device according to claim **1**, further comprising one or more of the deep layers, wherein

the deep layers are located at predetermined intervals.

4. The silicon carbide semiconductor device according to claim **1**, further comprising

a current diffusion layer located between the base region and the drift layer, wherein:

the current diffusion layer is made of silicon carbide and has the first conductivity type; and

the current diffusion layer has an impurity concentration greater than or equal to the impurity concentration of the drift layer.

5. The silicon carbide semiconductor device according to claim **4**, wherein

the trench penetrating the current diffusion layer to the drift layer.

6. The silicon carbide semiconductor device according to claim **4**, wherein

the deep layer penetrating the current diffusion layer and being in contact with the base region.

7. The silicon carbide semiconductor device according to claim **1**, wherein

the impurity concentration of the drift layer decreases in a direction from the substrate toward the base region.